

Applications of Silicon Carbide JFETs in Power Converters

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Abstract—Silicon carbide (SiC) JFET devices exhibiting normally-off characteristics have become commercially available, enabling their adoption into power supply products. In this paper, the synchronous rectification characteristics of SiC JFETs are investigated and their overall performance in single phase power factor correction (PFC) circuits is measured. Efficiency comparisons in a high efficiency telecommunications power supply demonstrate superior performance of 1200V SiC JFETs compared to 900V silicon MOSFETs. A minimal switch, high voltage PFC topology, requiring 1200V devices, is evaluated; however the slew rate of the SiC JFETs is insufficient to exceed the efficiency of other topologies.

Initial testing is conducted in a three-phase cycloconverter application. Different switching behaviour is observed with SiC JFETs than silicon MOSFETs. The effect is shown to be due to the JFET's lower output capacitance which also leads to reduced switching loss.

It is concluded that SiC JFETs perform at a similar level to 600V silicon MOSFETs and better than 900V MOSFETs, whilst being a 1200V device. These aspects, coupled with their ability to conduct in either direction make the SiC JFET particularly well suited to cycloconverter applications.

AC-AC Power Conversion; AC-DC Power Conversion; Efficiency; JFET; Power Factor Correction; Silicon Carbide

I. INTRODUCTION

Silicon carbide enhancement mode (EM) JFET transistors, exhibiting normally-off characteristics have become commercially available, creating new opportunities for power converter designs. The EM SiC JFETs offer a combination of high blocking voltage, low channel resistance and low capacitance, implying a high suitability for many power supply applications.

EM SiC JFETs have compared favourably to silicon IGBTs in single phase PFC booster circuits [1]. However at similar power levels, silicon MOSFETs are likely to also offer superior performance to IGBTs due to the voltage drop across their $R_{DS(on)}$ being lower than the saturation voltage of an equivalent IGBT. This study compares performance of modern high efficiency MOSFET implementation against SiC JFETs.

II. NORMALLY-OFF SILICON CARBIDE JFET CHARACTERISTICS

A. Reverse blocking voltage

Although the manufacturer provides little specific information regarding the nature of the SiC JFET's reverse conduction characteristics, synchronous rectification was observed in [2].

DC tests of a SemiSouth 1200V 15A SiC JFET[3] showed that the reverse channel resistance of the normally-off SiC JFET is similar to its forward characteristic when the gate-source voltage is well above the threshold voltage. Under gate-source short circuit conditions, the forward blocking voltage is in excess of 1200V[3], however reverse blocking ability is not mentioned. Tests demonstrated that the EM SiC JFET conducts well in the reverse direction under gate-source short circuit conditions, with only a small voltage drop across the channel. Application of a negative gate-source bias was found to result in an increase in the channel voltage drop of a similar magnitude, shown in Figure 1.

This unusual reverse blocking characteristic offers a distinct advantage because applying a small negative gate bias to the normally-off SiC JFETs allows them to block a reverse voltage greater than the forward voltage drop of an external anti-parallel diode, including SiC Schottky diodes which typically exhibit very high forward voltage drops. By forcing the conduction of an external diode, the EM SiC JFET body does not necessarily need to undertake any reverse conduction that may be required in an application. This allows an anti-parallel diode to be chosen independently of the transistor for optimum performance.

Silicon MOSFETs, in contrast, defeat the use of an external diode due to their particularly low body diode forward voltage drop. This forces a dependency between diode and transistor characteristics. Typically the body diodes of silicon MOSFETs exhibit very poor reverse recovery characteristics, limiting the switching speeds in hard-switched constant inductor current applications.

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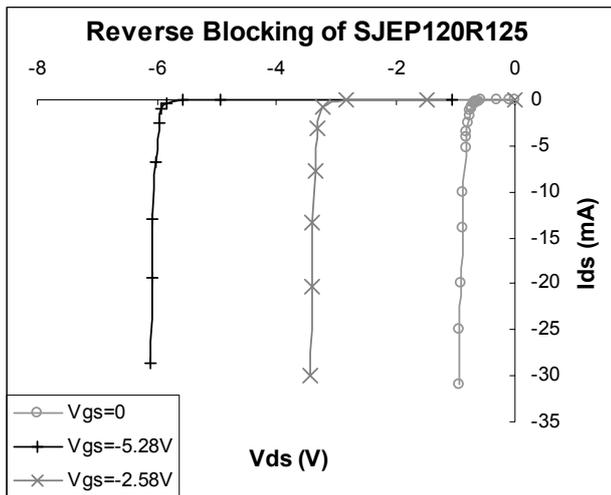


Figure 1: SiC JFET reverse blocking characteristics

B. Reverse Recovery

While correctly driving the EM SiC JFETs can force an external diode to carry reverse currents, characterisation of the JFETs' own reverse recovery behaviour is useful in determining the necessity of such an external diode.

The reverse recovery characteristics of the SiC JFET were measured using a method similar to [4] and [5]. Other devices were also subjected to the same test to facilitate a meaningful comparison. The results are summarized in Table I.

TABLE I. REVERSE RECOVERY TIMES FOR SiC JFET COMPARED TO OTHER DEVICES

Device	$T_a(ns)$	$T_b(ns)$	$T_{rr}(ns)$
SiC JFET	18.0	20.0	38.0
Si MOSFET (600V)	140.0	29.3	169.3
Si Hyper-fast diode	14.6	9.9	24.5
SiC Schottky diode	13.6	9.1	22.7
SiC JFET & SiC diode	23.0	22.9	45.9

The reverse recovery time of the SiC JFET was found to be significantly smaller than that of the silicon MOSFET. In combination, a SiC JFET and SiC diode also achieved far superior reverse recovery times than those exhibited by the silicon MOSFET. **The lack of any performance advantage being achieved in this test by the addition of an anti-parallel diode to the EM SiC JFET, suggests that such an external diode is likely to be unnecessary in a majority of applications.**

C. Self-powered split JFET driver

Initial experimentation with typical MOSFET drive circuits has demonstrated that shoot-through can easily occur when the EM SiC JFETs are used in a bridge leg topology. The problem has been observed previously and precautions taken to prevent

it, as well as to achieve optimum switching speeds[1]. However, the solution proposed in [1] requires a split 15 volt supply, not typically found in existing MOSFET based power converters. For ease of adoption, it is preferable for such a driver to operate from a single 7-10V supply rail and be constructed in the form of an application specific integrated circuit (ASIC). To meet these specifications, a new JFET driver circuit is proposed that derives its negative voltage rail by way of a charge pump. The prototype is also constructed from similar sub-circuit building blocks to those commonly found in MOSFET driver ASICs. These include logic gates, delays, Schmitt triggers, level shifters, Schottky diodes and high current output stages.

The proposed drive circuit is shown in Figure 2, driving a bridge leg topology. It utilizes a separate dual MOSFET driver IC for each JFET. Both drivers and all logic circuitry (not shown) could be incorporated into a single ASIC.

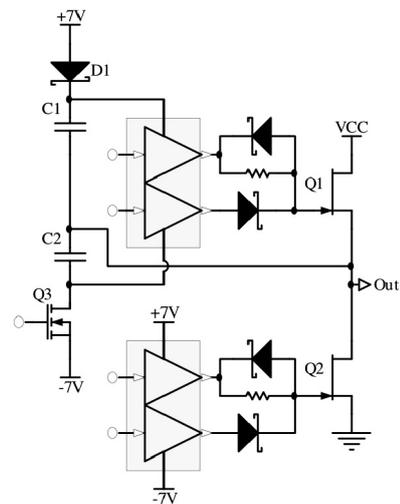


Figure 2: Proposed JFET driver topology

The lower half of each driver is driven with a short pulse to generate a brief high current pulse into the JFET gate, ensuring rapid turn-on. Meanwhile, the upper half provides the necessary continuous current required to maintain a turned-on state. The upper half of the driver also provides a low impedance current sink to rapidly facilitate and sustain transistor turn-off.

The driver ICs are operated from split supply rails similar to [1], however the negative supply rail in the prototype is derived internally from the positive rail by way of a charge pump. Thus, only a single supply rail is required. The voltage of the supply rail can be anywhere in the range of 7-10V, typically available in existing power converter products.

D1, C1, C2 and Q3, allow the floating high side driver to be powered by a bootstrap circuit. When Q2 is on, C1 automatically charges, analogous to many MOSFET driver bootstrap arrangements. However, by turning on Q3, C2 is also allowed to charge. Thus, both the positive and negative

rails are level shifted as required to drive the upper EM SiC JFET in the bridge.

The proposed drive topology requires one constraint to be met that is not present in common MOSFET driver circuits. That is the requirement for Q3 to be turned off before Q2. With small delays and logic gates, this constraint is easily met. The addition of a Schmitt trigger to the output node can provide an additional failsafe by ensuring that Q3 cannot turn on until the node has dropped to less than 1 volt above ground.

Although the EM SiC JFET possesses a higher Miller to input capacitance ratio than modern high efficiency silicon Superjunction MOSFETs, shoot-through is still seen with silicon devices. In [6], shoot-through is observed in an insulated gate bipolar transistor (IGBT) based bridge circuit and a small negative gate voltage is utilized to mitigate the issue. The solution proposed introduces an additional lossy component into the load current path, significantly increasing circuit losses. It is further proposed in [6] that the device be a MOSFET to allow the losses to be reduced through synchronous rectification. The drive circuit proposed in Figure 2 does not require any device to be added to the load current path and can thus provide a good solution for the IGBT application.

III. BRIDGELESS SINGLE PHASE BOOSTER APPLICATION

The SiC JFET is considered for use in a single phase power factor correction (PFC) boost circuit that draws a unity power factor current waveform from a 230V utility and drives a constant power load. The topology, shown in Fig. 3, has a distinct conduction loss advantage over many other topologies by having only one active device conducting current at any time. The classic boost converter has a full bridge resulting in two diode drops, followed by a third voltage drop across the switch or rectifier. Modern high efficiency PFC topologies achieve a reduction of one voltage drop by combining device functions. Having only one device in the current path could offer a further substantial reduction in conduction losses.

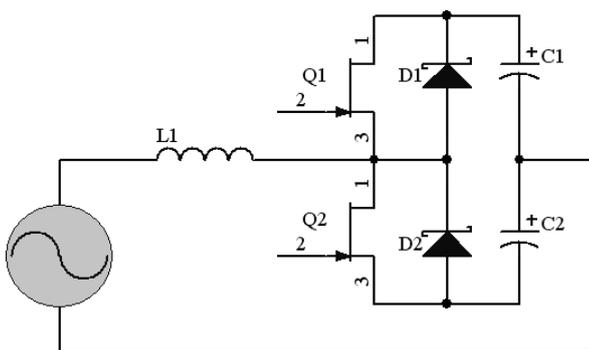


Fig. 3: Proposed minimal switch PFC circuit

The caveat of the proposed topology is that it requires its transistors to withstand twice the voltage of other topologies, preventing it from being implemented with 600V MOSFETs.

Furthermore, a quantity of energy flows reactively between the two output capacitors, resulting in an increase in conduction losses compared to a standard boost converter topology. Extensive modelling has shown that the increase in losses is insignificant compared to the advantage of having only one device voltage drop.

The topology has been used in uninterruptible power supplies (UPS) [7], where IGBTs are commonly used to achieve the necessary voltage ratings while switching is performed at relatively low frequencies of several kHz. In UPS installations, audible noise and physical size can be tolerated through carefully designed plant rooms. The high speed and 1200V blocking capabilities of the EM SiC JFET enable this topology to be considered for other applications where it is crucial to keep switching frequencies in the tens to hundreds of kHz.

Telecommunications rectifiers are also well suited to the topology. However, they have even stronger requirements on switching frequency. Physical size is a major constraint in roadside equipment cabinets for legislative reasons. The switching frequencies must also be kept high to avoid compromising the audio quality of telephony systems.

Performance of the booster circuit was evaluated mathematically under both best and worst case scenarios. Best case scenario assumes a low transistor temperature and zero drain-source voltage at the turn-on instants when operating in discontinuous conduction mode (DCM). The worst case assumes a high transistor temperature and full bus voltage appearing across a transistor at the turn-on instant. In practice, the turn-on voltage under DCM varies with load, switching frequency and parasitic elements, causing the actual performance to vary between the two scenarios. At higher loads, the converter enters continuous conduction mode and the difference between worst and best scenarios becomes very small. This is because the transistors always experience the full bus voltage across them while turning on.

A prototype of the DC equivalent circuit was constructed to test the circuit model at discrete operating points in the 230V single-phase mains supply cycle. A two stage gate driver, similar to that in [1] was utilized for optimum switching performance. The efficiency performance of the prototype is shown in Figure 4, where the expected variations in the DCM region can be clearly seen as sinusoidal deviations in efficiency.

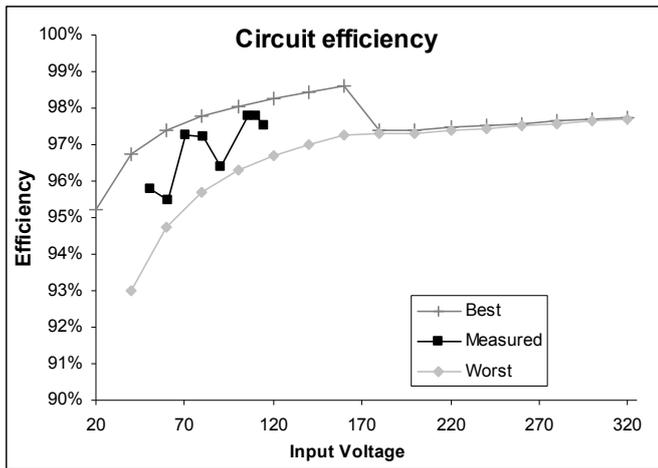


Figure 4: Performance of the PFC circuit; power proportional to square of voltage

The results verify the accuracy of the model under DCM; however limitations in the test prototype limit results to DCM only. Modelling of aggregate circuit efficiency demonstrated that although giving high efficiency, the topology is unable to rival the efficiency of other topologies which are able to use modern high efficiency 600V silicon Superjunction MOSFETs. This is because the proposed topology requires twice the voltage to be switched compared to other topologies. For switching losses to remain equal, the two times higher voltage must be slewed in a shorter period of time. This equates to a slew rate several times higher than required in alternative topologies. In practice, the slew rate of the EM SiC JFET is similar to that of the best 600V silicon MOSFETs, falling short of the requirement. As EM SiC JFET technology improves over time, this topology is likely to become a suitable choice for PFC circuits.

IV. REAL WORLD POWER SUPPLY APPLICATION

To compare the EM SiC JFET directly with silicon transistors in a real world scenario, a commercial telecommunications rectifier product was selected. The rectifier product has a single phase PFC boost circuit at its input, whose underlying topology is shown in Figure 5. With minor modifications to the gate drive circuits, the MOSFETs were replaced with EM SiC JFETs.

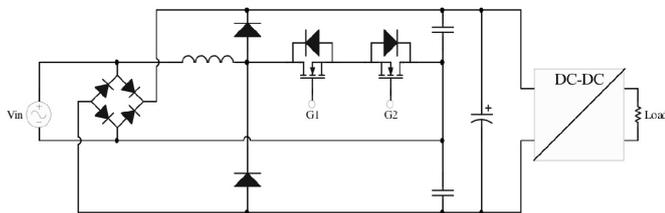


Figure 5: Topology of the telecommunications rectifier product's PFC stage

Performance of the converter was evaluated by measuring the input and output power of the entire converter, including the unmodified filtering and DC-DC converter stages. The input power was measured using a high accuracy, calibrated AC

power meter and the output power was measured using a calibrated, temperature controlled DC shunt. The input voltage was maintained within a one volt R.M.S. range at all times. A computer based data acquisition system sampled and averaged several measurements for each data point, time-synchronized with each other and the mains.

For comparison purposes, the same hardware and measuring equipment was used to test 600V and 900V silicon transistors. The test results are shown in Figure 6.

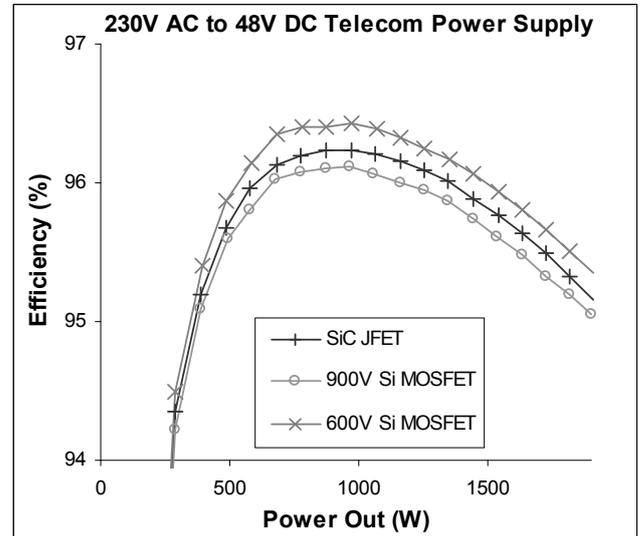


Figure 6: Performance of EM SiC JFET against silicon MOSFETs in a real-world application

The 1200V SiC JFETs achieve higher conversion efficiency than modern high efficiency 900V silicon MOSFETs, in addition to possessing a superior breakdown voltage.

600V silicon MOSFETs outperformed the 1200V EM SiC JFETs by a small margin of 3.99W at the maximum load of 2kW and 1.9W at 1kW. These differences represent 0.2%, suggesting that the EM SiC JFET performs on par with 600V silicon MOSFETs, whilst being capable of blocking 1200V.

At very low load, performance between the three devices is even closer, diverging with increasing load. This suggests that conduction losses are likely to be the dominant component as it is more heavily dependent on current than switching losses are. Close inspection of manufacturers' specifications reveal that the 600V silicon MOSFET and 1200V SiC JFET exhibit very similar channel resistances at 25°C. However, despite being packaged in the same style of casing, the junction to case thermal impedance of the EM SiC JFET is more than double that of either the 600V or 900V silicon MOSFET. This is due to the EM SiC JFET's significantly smaller die. The EM SiC JFETs were tested in the same circuit as the silicon MOSFETs (electrically and thermally), their higher thermal impedance causing them to operate at a higher temperature. The higher operating temperature in turn increased the conduction losses, leading to further temperature increases in a positive feedback cycle until thermal equilibrium was reached.

The net results were higher conduction losses in the 1200V EM SiC JFET than the 600V silicon MOSFET.

The thermal constraint is clearly one of the EM SiC JFET's largest shortcomings. At the same time, the small die is responsible for the EM SiC JFET's cost effectiveness.

V. THREE PHASE CYCLOCONVERTER

Findings from tests conducted on single phase converters motivated the investigation of potential three-phase applications for the EM SiC JFET. Because the EM SiC JFET can conduct in either direction, it is suitable for three-phase cycloconverter applications such as the topology shown in Figure 7.

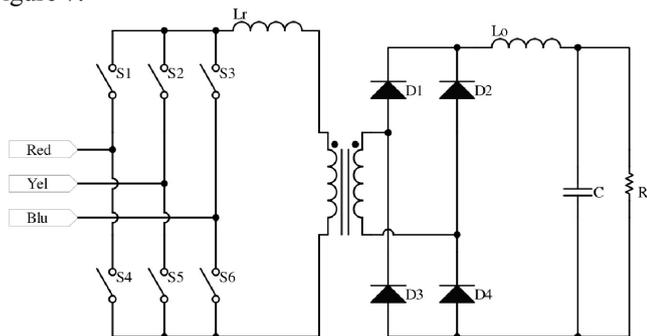


Figure 7: Three-phase cycloconverter topology

The topology relies upon six bidirectional switches, each of which is constructed from a pair of back-to-back MOSFETs to enable blocking to be performed in either direction. During part of the switching sequence described in [8] as being equivalent to the "Bridge Y" sub-topology, a prototype behaved differently when EM SiC JFETs were used in place of silicon MOSFETs. The applicable portion of the mains cycle is shown in Figure 8(a). Initially, current flows from the red phase to the blue phase via S1 and S6. They then turn off and switches S3 and S4 turn on, as shown in Figure 8(b), to facilitate current flow in the opposite direction -from the blue phase to the red phase.

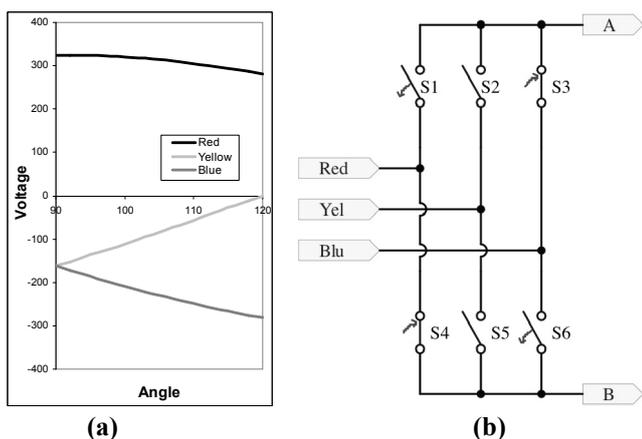


Figure 8: Subset of the switching cycle (a) where the voltages across S2 and S5 change polarity when the other switches change state (b)

During the transition between these two modes of operation, switches S2 and S5 remain off, blocking any differences in voltage between the yellow phase and points A and B. Before the transition, node B is at the same potential as the blue phase and switch S5 must block the yellow-blue line-to-line voltage, shown as V_{S5} in Figure 9(a), where the individual MOSFETs that make up S5 are shown. After the transition, node B is at the same potential as the red phase and switch S5 experiences the yellow-red line-to-line voltage shown as V_{S5} in Figure 9 (b). V_{S5} changes magnitude and polarity between the two modes and the blocking of V_{S5} during these two modes is performed by transistors S5a and S5b respectively.

When S5 is built from two EM SiC JFETs however, the change in polarity and magnitude of V_{S5} does not result in a perfect handover from S5a to S5b. Similarly to MOSFETs, switch S5 begins with its upper JFET S5a blocking V_{S5} as shown in Figure 9(c); upon the reversal of polarity of V_{S5} , the voltage across transistor S5a decreases to a smaller value V_X and the voltage across S5b increases to V_Y , the sum of V_X and V_{S5} as shown in Figure 9(d). S5a and S5b are thus blocking larger voltages than expected because the midpoint between them is more negative than either end of the bidirectional switch that they form.

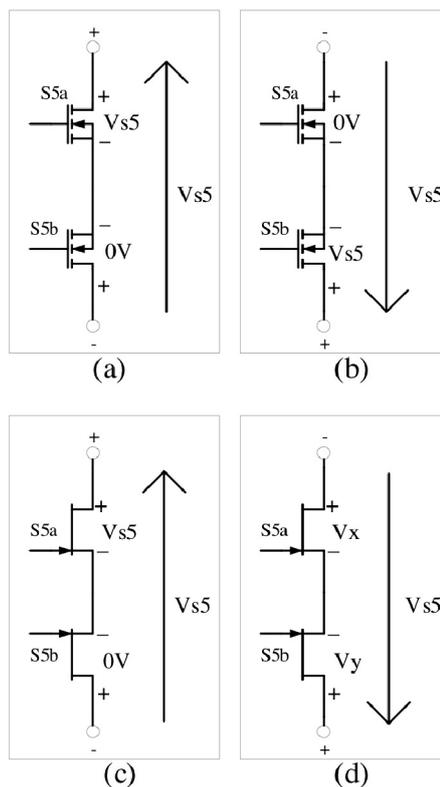


Figure 9: Switch S5 before and after the V_{S5} polarity reversal when constructed from silicon MOSFETs (a) & (b) and EM SiC JFETs (c) & (d)

The transition involves current flowing through the output capacitances of the transistors, discharging C_{S5a} and charging C_{S5b} . Like a silicon MOSFET, the output capacitance of an

EM SiC JFET increases at low voltages. The 1200V EM SiC JFET's output capacitance was quoted as being approximately 90pF at a drain-source voltage of 100V.[3] Without any drain-source potential, this capacitance was found to increase to 800pF at zero volts. In comparison, the silicon MOSFET originally used in the cycloconverter was quoted as having an output capacitance of 330pF[9] at a drain-source voltage of 100V and found to have a value of 53.7nF at zero volts.

In the case of the silicon MOSFET, the large output capacitance of S_{5b} before the transition ensures that the smaller capacitance in S_{5a} fully discharges. In the EM SiC JFET, the output capacitance increases by a smaller proportion at zero volts. This results in the capacitance of S_{5a} being too small to fully discharge the transitions because the voltage across the pair of transistors after the transition is of lesser magnitude than and opposite polarity to what it was before.

The reason that such a large capacitance is required for S_{5b} relative to S_{5a} , in order for a complete transition to take place, is that the voltage after the transition has a smaller magnitude than the one before. Each switch is affected by this phenomenon during some period of a mains cycle, by symmetry.

Whilst the phenomenon involves higher voltages being developed across the EM SiC JFETs than silicon MOSFETs during a specific subset of the switching sequence, the significantly smaller capacitance that causes this effect is also responsible for less energy being stored. Reduced energy storage leads to an improvement in switching losses and therefore conversion efficiency.

The highest voltage observed in this scenario was shown mathematically to never exceed the highest voltage normally experienced at any other time during a mains cycle. Thus, the phenomenon does not threaten to cause excessive voltage stress to the devices.

VI. CONCLUSIONS

The EM SiC JFET was shown to offer full flexibility in the choice of anti-parallel diode characteristics, a liberty not afforded with silicon MOSFET devices. The reverse recovery of the SiC JFET itself was also found to be significantly faster than that of silicon MOSFETs, removing the motivation to use a fast external anti-parallel diode. The SiC JFET is thus well suited to high-speed synchronous rectification and bidirectional switching applications where the reverse recoveries of silicon MOSFET body diodes typically limit switching performance.

Performance of the EM SiC JFET was evaluated and tested in a single phase PFC application that allows the JFET's high voltage and speed characteristics to be utilized. However efficiency was not found to exceed that achieved by state of the art topologies. This is because the blocking voltage,

experienced by the devices in the high voltage application, dictates that the transistors be several times faster than lower voltage devices in alternative topologies, for the potential performance of the topology to be realized.

The high blocking voltage of the EM SiC JFET makes it particularly suited to three-phase bidirectional switching applications, where silicon devices with ratings of at least 900V are typically used. EM SiC JFETs were tested in a three-phase cycloconverter application. Here, different switching behaviour was observed to that of silicon MOSFETs, however it was shown that the behaviour does not compromise the operation of the converter. The JFETs' output capacitance was found to be significantly smaller than that of comparable silicon MOSFETs, suggesting that lower switching losses are likely to occur.

The EM SiC JFET was shown to offer similar performance to state-of-the-art 600V silicon MOSFETs and superior performance to 900V silicon MOSFETs whilst itself possessing a breakdown voltage of 1200V. These characteristics make it a good device to consider for three-phase power converter applications.

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