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Silicon carbide JFET reverse conduction characteristics and use in power converters

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Abstract: Recent advances have resulted in the availability of a new generation of silicon carbide (SiC) junction field effect transistors (JFETs), which unlike previous generations, exhibit highly desirable normally off characteristics. Normally off SiC JFETs are characterised with particular focus on previously unknown reverse conduction characteristics. Refinements are proposed to JFET gate driving circuits that allow their implementation as a single-chip solution. Reverse recovery characteristics of SiC JFETs were measured using diode testing techniques and found to be significantly faster than typical silicon metal oxide semi-conductor field effect transistor (MOSFET) body diodes. SiC JFETs are compared with silicon MOSFETs in power factor correction boost converters, including a real-world application where superior power conversion efficiency utilising SiC JFETs is demonstrated.

1 Introduction

Recent advances in silicon carbide (SiC) semi-conductor technology have led to the development of a range of SiC transistors. One of the more promising devices has been the SiC JFET. Usually, under zero gate-source voltage conditions, JFETs exhibit normally-on characteristics making them difficult to utilise in power converters because of fail-safe and start-up requirements. Various techniques have been devised to overcome these issues such as cascode topologies [1, 2]. Recently, enhancement mode (EM) SiC JFETs have been developed that exhibit normally-off characteristics [3] using the structure shown in Fig. 1 [4]. These normally-off characteristics allow for simpler implementations because of their inherent fail-safe attributes.

Characteristics of the EM SiC JFET have been provided in [5, 6]. However, little is known about this device's characteristics when the polarities of drain–source currents and voltages are reversed. Here, a range of previously unknown reverse polarity characteristics of the EM SiC JFET are measured, including blocking ability, conduction and reverse recovery. These characteristics allow EM SiC JFETs to be evaluated for their suitability in several power converter applications. Several relevant real-world applications are identified and their performance with EM SiC JFETs is measured by constructing prototypes and retrofitting commercial power converters. The reverse characteristics of EM SiC JFETs described in this paper are of significant value when designing power converters that require current to flow in both directions through an EM SiC JFET.

2 Enhancement mode SiC JFET

The EM SiC JFET tested is capable of blocking 1200 V between its drain and source terminals in the presence of a gate-source short-circuit [3]. Unlike the EM silicon power metal oxide semi-conductor field effect transistor (MOSFET), the EM SiC JFET does not contain a parasitic body diode [7]. In a variety of applications such as high-frequency synchronous rectification (SR), a fast body diode reverse recovery is needed for high conversion efficiency to be achieved [8]. The EM SiC JFET's lack of a body diode therefore has important performance implications that are quantified with a number of tests.

2.1 Gate drive

Most JFETs require a negative gate–source potential in order to prevent current from flowing through the device channel. The EM SiC JFET is capable of blocking 1200 V without a negative gate–source potential, while exhibiting a relatively small leakage current. In [3], the drain leakage current is stated for both $V_{gs} = 0$ V and $V_{gs} \leq 15$ V conditions, suggesting that a negative gate–source voltage does have an effect on the EM SiC JFET.

The EM SiC JFET is a voltage controlled device and a conducting state is maintained by the application of a positive gate–source voltage. When such a voltage is

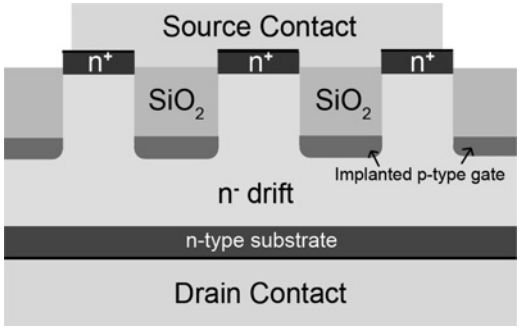

Fig. 1 *Cross-section of the EM SiC JFET*

present, current flows through the gate–source junction of the EM SiC JFETs and thus contributes to overall losses. To achieve the highest possible conversion efficiency, a compromise must be made between drive losses and conduction losses. The gate drive circuit design also affects the speed at which the EM SiC JFET switches on and off, resulting in an additional compromise between drive losses and switching losses.

To quantify drive losses, the EM SiC JFET is tested under constant gate voltage conditions to observe how much gate current is drawn over a broad range of both positive and negative drain–source currents. The gate current is then limited, effectively capping the drive losses while conduction losses are measured to identify what drive conditions are likely to achieve the optimum compromise.

2.2 Negative gate bias

In half-bridge topologies, shoot-through problems have been observed by the authors as well as in [7, 9]. It was identified in [7] that the shoot-through problems occur because of a high Miller capacitance to input capacitance ratio and that the substitution of a negative gate–source voltage in favour of a short circuit during turn-off mode is an effective method for solving this problem.

The requirement of a bipolar drive, capable of delivering sustained gate current necessitates the design of a specialised driver circuit. Suitable drive circuits have been explored in [7, 10] which fulfil these requirements and deliver good performance. These designs operate from a bipolar power supply, which is not typically available in commercial power converters, necessitating significant changes to auxiliary power supply designs.

2.3 Synchronous rectification

In [9] SR was observed with EM SiC JFETs, demonstrating the possibility of this mode of operation. Although SR was shown to offer a reduction in conduction losses, the reverse recovery performance was not considered. Reverse recovery can pose a performance problem because a short dead time is typically needed in hard-switched applications [11]. During this dead time, the SR MOSFET is effectively turned off prematurely, causing its body diode to conduct briefly and then experience reverse recovery at the actual transition. The issue has influenced the design of MOSFETs for SR applications [8, 12] and prompted the development of sophisticated techniques for minimising dead time [13]. Since the EM SiC JFET does not possess a body diode [7], it is unclear what its SR performance is likely to be.

The possibility of reverse conduction alone does not guarantee outstanding performance in high-frequency SR applications, because the reverse recovery behaviour of the transistor has a major effect on switching losses. Silicon MOSFET body diodes typically exhibit extremely poor reverse recovery behaviour, leading to particularly significant switching losses. Although the EM SiC JFET contains no body diode, parasitic capacitances will cause some degree of reverse recovery-like characteristics, which need to be quantified in order to accurately model performance.

3 Power factor correction applications

Active power factor correction (APFC) circuits are used in many single-phase power converters to achieve a high-power factor. The classic APFC topology is simply a full-bridge rectifier followed by a boost converter. This topology exhibited superior efficiency when using EM SiC JFETs in place of silicon IGBTs in [14]; however, comparisons were not made to silicon MOSFETs. The super-junction silicon MOSFET is often used in modern power converter PFC circuits and should also be considered as a competing device when evaluating SiC JFETs.

To achieve the biggest reductions in power loss, the APFC topology itself must be evaluated in addition to the choice of transistor. In the classic APFC topology, whether the transistor is on or off, current must always flow through a total of three semi-conductor devices: two rectifier diodes and either the transistor or fast rectifier diode. A consequence of having current flowing through three semi-conductor devices is a significant conduction loss. These losses have increased the popularity of several other topologies that do not require as many semi-conductor devices to conduct in series. Many recent APFC topologies increase conversion efficiency by dispensing with the diode bridge through the combination of the rectification and boost functions. The result is a bridgeless APFC circuit where current typically flows through two semi-conductor devices at any time, instead of three, resulting in reduced conduction losses [15–17]. The minimum requirement for two series devices in these topologies typically arises from the need to provide bidirectional blocking.

A topology that only carries current through one semi-conductor device at any time is shown in Fig. 2. The trade-off in this topology is that the voltage which must blocked by each transistor is double that of many other topologies. Typical 230 V single-phase utility supplied APFC circuits provide a 400 V DC output and thus are able to choose from the broad range of high performance 600 V MOSFETs to meet this requirement. The topology in Fig. 2 must block 800 V, rendering 600 V MOSFETs unsuitable.

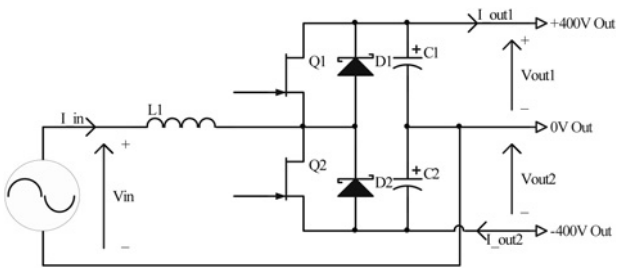

Fig. 2 *APFC topology with single semi-conductor device in each current path*

EM SiC JFETs rated at 1200 V easily block the 800 V in this topology.

3.1 Modelling

3.1.1 Overview: The topology proposed in Fig. 2 was modelled by mathematically calculating a number of operating points in a mains cycle. By approximating the losses of each circuit element at each point, an overall efficiency figure was calculated.

A number of output loading arrangements are possible with this topology. One arrangement, believed to result in optimum efficiency is where the load is shared by two DC–DC converters. One converter is supplied from C1 and the other from C2. By modulating the two converters, it is possible to draw the full-load power from C1 during positive mains half-cycles and C2 during negative half-cycles. This maximises the efficiency of the boost converter by minimising the amount of energy storage that occurs.

3.1.2 Operating points: The PFC circuit is modelled at an input power of 2 kW from 230 V_{rms}. To achieve unity power factor at an average power of 2 kW, the input current is kept in direct proportion with input voltage. At full load of 2 kW, the circuit converts 4 kW at the 325 V peak of the AC input. An important characteristic of the topology in Fig. 2 is that energy circulation occurs between C1 and C2. During positive half cycles, Q2 acts as the boost switch, whereas Q1 and D1 act as rectifiers. During this time, C1 is charged and C2 is partially discharged. By symmetry, Q1, D1 and C1 switch roles with Q2, D2 and C2 during negative half-cycles.

During positive half-cycles, the APFC circuit in Fig. 2 is similar to the classic boost converter, except that the voltage across C2 appears in series with the input voltage when Q2 is on. This has the effect of reducing the duty cycle of Q2, resulting in the relationship in (1), where v_{in} is the instantaneous mains input voltage, v_{C1} is the voltage across C1, v_{C2} is the voltage across C2 and D is the duty cycle of Q2.

$$\frac{v_{C1} - v_{in}}{v_{in} + v_{C2}} = \frac{D}{1 - D} \tag{1}$$

In a classic boost converter, there is no C2 capacitor and thus $V_{C2} = 0$; and (1) then simplifies to the familiar relationship in (2).

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 - D} \tag{2}$$

At low input currents, the APFC operates in discontinuous conduction mode (DCM). The voltage across Q2 at the turn-on moment varies under DCM between zero and $V_{C1} + V_{C2}$, resulting in a variation in switching losses. Since the exact voltage across Q2 at turn-on is dependent on input voltage, load, V_{C2}, the inductances and capacitances of L1, Q2, Q1, D1 and the physical circuit layout itself, two models are proposed. The first model considers the best case scenario where $V_{DS(Q2)}$ is zero at turn-on, resulting in zero voltage transition turn-on. The second model considers the worst case scenario where $V_{DS(Q2)}$ is equal to $V_{C1} + V_{C2}$ at turn-on. The latter scenario always applies when the circuit operates in continuous conduction mode (CCM).

3.1.3 Capacitor losses: To model the losses in the capacitors, the equivalent series resistances (ESRs) of the components are used. Under DCM, when Q2 turns on, the current through Q2 and C2 rises linearly from zero to some peak value I_{pk}, reached when Q2 turns off. Given the triangular wave-shape of the capacitor current over this time period, the RMS value of the current is expressed as (3).

$$I_{rms} = \frac{I_{pk}}{\sqrt{3}} \tag{3}$$

If D is the duty cycle (of Q2) and R_{C2} is C2's ESR, the power dissipated by C2 can be represented by (4).

$$P_{C2} = \frac{I_{pk}^2}{3} D R_{C2} \tag{4}$$

During CCM, the inductor current is always non-zero. The average inductor current is a function of input voltage and power and thus easily derived. If it is assumed that the voltage across C2 remains approximately constant, the duty cycle can be calculated. By knowing the chosen switching frequency, the linear rise in inductor current while Q2 is on can be calculated.

Having defined the current through C2, the resulting losses are estimated by splitting the current into two parts, a 100 Hz component and a switching frequency component. The 100 Hz component is caused by (and calculated from) the imbalance between the constant output power supplied from the 400 V bus and the sinusoidal input power drawn from the mains. The balance of the current through C2 is the switching frequency component. This switching frequency component is generated by the rapid toggling between the two conduction modes.

The capacitor proposed for use in a prototype converter for each of C1 and C2 is constructed from the parallel combination of two 180 μF electrolytic capacitors and two 680 nF polyester capacitors. The electrolytic capacitors provide bulk capacitance and low ESR at 100 Hz while the polyester capacitors provide low ESR and inductance at high frequencies. The proposed compound capacitor's ESR was measured using a Wayne Kerr 3260B precision magnetics analyser. The ESR was found to be 124.7 m Ω at 100 Hz and 17.2 mΩ at 120 kHz. The significantly lower high-frequency ESR is achieved by design, and is implemented because of the high-frequency component of the current through C2 being significantly larger than the low-frequency component.

3.1.4 Transistor conduction losses: The channel resistance of each transistor is assumed to be equal to that of the other transistor because of their thermal time constants being significantly slower than the 20 ms period of the sinusoidal input current. Since the junction temperature has an interdependent relationship with the channel resistance, small variations in current, temperature or channel resistance will result in larger variations in channel resistance and temperature. To encompass a broad range of possibilities, the worst case model uses an approximation of the drain current dependent data in [3] at the pessimistic junction temperature of 150°C, whereas the best case model uses the highly optimistic 25°C data. Under the poorest conditions, the worst case model gives a channel resistance of 0.25 Ω at 150°C.

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At low currents, SR is used in Q1 to reduce conduction losses. At higher currents, the voltage drop across D1 is lower than the channel voltage drop of Q1 and SR does not occur. Whether rectification losses occur in D1 or Q1 affects the temperatures of Q1 and D1. The best and worst case models accommodate either thermal scenario satisfactorily because of their significantly different transistor temperature assumptions.

The actual rectification losses are found by assuming that SR occurs and calculating the losses in Q1, then assuming that SR does not occur and calculating the losses in D1. The lesser of the two cases is used as the authoritative model of rectification loss in the converter at a particular operating point.

3.1.5 Transistor switching losses: Switch-on losses for Q2 are assumed to be zero in the best case scenario during DCM because of turn-on occurring under zero voltage conditions. The worst case model (and the best case during CCM) uses an approximation of the switching energy data in [3] to achieve an estimate of switching losses that is dependent on drain current. The average inductor current is used for this parameter and the losses are scaled to compensate for the minor difference in voltage between [3] and this application.

3.1.6 Inductor losses: Inductor losses are calculated based on the inductor's winding resistance, which were measured at 50 Hz using a Wayne Kerr 3260B precision magnetics analyser. The inductor proposed for use in a prototype converter has a measured inductance of 122 μH and exhibited a measured ESR of 80.1 mΩ, allowing the copper losses to be calculated.

The inductor is wound with Litz wire and was found to only exhibit a small increase in resistance at 120 kHz because of skin and proximity effects. The worst case circuit model uses a larger inductor winding resistance to take into account the increased resistance for the high-frequency ripple current as well as some rise in resistance because of elevated temperature.

4 Device characterisation

4.1 DC tests

SJEP120R125 SiC JFETs in TO-247 cases [3] were used in all evaluations. Transistors were thermally connected to large heat sinks with forced air cooling to minimise heating effects. Measurements were taken only after thermal equilibrium was attained, to minimise transient thermal effects.

To characterise the EM SiC JFET in the absence of any gate drive, the gate and source terminals were short-circuited while current was allowed to flow through the body in the source-to-drain direction. The body voltage drop was monitored across a broad operating range and is presented in Section 5. To observe the effects of biasing, the tests were repeated with several voltage and current sources applied to the EM SiC JFET's gate–source junction.

4.2 Gate drive losses

Since the EM SiC JFET requires a continuous gate current to maintain a forward conducting state [7], drive losses need to be accounted for. The EM SiC JFET was provided with a voltage source gate-bias arrangement and the gate current monitored across a range of operating conditions to evaluate the gate drive power requirements.

To more accurately model a likely gate drive arrangement, the EM SiC JFET was also biased from a current-limited voltage source. The drain–source voltage drop was observed over a broad range of operating conditions to evaluate the effects of a current limit on conduction performance.

4.3 Rectification performance

To evaluate the switching performance of the EM SiC JFET as a passive diode, current was allowed to flow in the source-to-drain direction under gate–source short-circuit conditions. The current was then rapidly interrupted by the application of a large positive drain–source voltage. This method is based on the reverse recovery test outlined in [18].

The results were obtained by monitoring the voltage and current with an oscilloscope. Circuit layout best-practices were followed and a 100 MHz Tektronix TCP312 current probe was utilised to measure the current. Before testing commenced, a high-frequency AC signal and low-inductance resistor were used to calibrate the skew of the current and voltage probes.

To allow a meaningful comparison to be made, the same test was performed on silicon MOSFETs, SiC JFETs, a variety of diodes and combinations thereof. By using the same test circuit for all devices, side-by-side comparisons are possible.

4.4 Gate driver design

The voltage required to turn-on the EM SiC JFET is considerably smaller than the 15 V used in [19], as is the negative voltage required to prevent shoot-through. It is proposed that an EM SiC JFET gate drive circuit should operate from a single 8–10 V supply rail, similar to those already typically present in the auxiliary power circuits of many commercial power converters.

It is further proposed that an EM SiC JFET gate drive circuit be manufactured as an application-specific integrated circuit (ASIC), forming a single-chip solution to driving EM SiC JFETs. The proposed EM SiC JFET gate drive circuit shall therefore be designed from the same building blocks present in commercially available MOSFET driver ASICs.

A simplified representation of the proposed gate drive circuit is shown in Fig. 3 configured for a half-bridge inverter application. Each EM SiC JFET is driven by a pair of low output impedance power stages. One stage in each pair delivers brief pulses of current at turn-on via a diode, whereas the other stage provides a continuous gate current limited by a resistor. The resistor is reverse bypassed by a diode to achieve rapid turn-off and maximum shoot-through immunity.

Power consumption from the negative supply rail is small because a sustained negative gate current does not flow. This allows the negative supply rail to be generated by a simple capacitor charge-pump circuit (not shown) as demonstrated in [20]. The positive supply rail for the upper JFET's gate drive stages is bootstrapped with the same topology commonly used for MOSFETs. The constant gate current requirement increases the demands placed on the bootstrap circuit compared with those for driving a silicon MOSFET. Voltage ripple can be maintained at a suitably low level by increasing the capacitance of C1. A simple

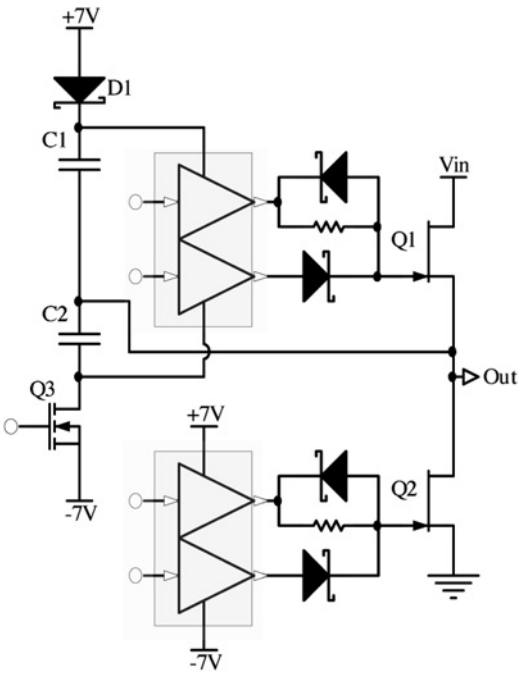

Fig. 3 *Proposed JFET driver circuit overview*

scenario was simulated where C1 is initially charged to 7 V and then connected to the SiC JFET via an 18 Ω gate resistor. With a duty cycle of 95% and a switching frequency of 100 kHz, a capacitance of ~1 uF was needed for C1 in order to maintain a gate current of at least 100 mA for the entire 9.5 μs. 1 uF is significantly larger than the values typically used in MOSFET circuits, but not so large as to be impractical.

The negative voltage rail for the upper JFET's gate drive stages is also level shifted via a bootstrap arrangement. The charging of this bootstrap is achieved by turning on Q3 for a subset of the time that Q2 is on. If Q3 is turned on while Q2 is off, C2 will charge to 7 V greater than VCC, destroying the upper JFET drivers.

To demonstrate the feasibility of the drive signals required by the proposed driver, a prototype circuit was constructed from several logic gates and passive components. From a single pulse width modulation (PWM) input signal, the prototype generated the three required logic signals for the three transistors in Fig. 3. The logic circuit incorporates a hysteretic lockout that prevents Q3 from being on if the output voltage from the bridge is greater than one volt. This decreases the circuit's dependency on an accurately calibrated dead time.

5 Results

5.1 Reverse blocking

Under gate–source short circuit conditions, the EM SiC JFET conducts current in the source–drain direction. As shown in Fig. 4, the characteristic is neither purely ohmic nor like that of a diode.

The source-to-drain voltage drop observed with current flowing through the EM SiC JFET channel in the source-to-drain direction decreases when a positive gate–source voltage is applied (SR). When a negative gate–source voltage is applied, the channel voltage drop was found to increase. Observations over a range of gate–source voltages with light drain currents suggested that the source–drain

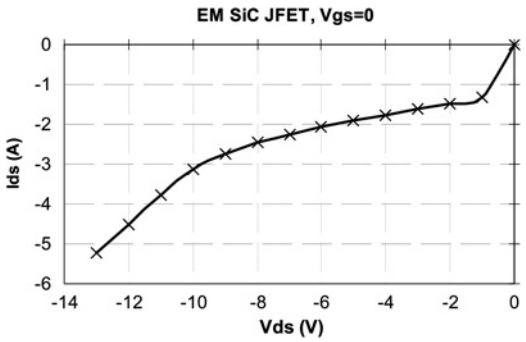

Fig. 4 *SiC JFET reverse blocking characteristic*

voltage drop is typically about 0.5 V larger than any applied negative gate–source voltage.

5.2 Gate drive power

When a fixed voltage is applied across the gate–source junction of the EM SiC JFET, the gate current drawn varies depending on the drain current. The characteristic is shown in Fig. 5 with a particularly steep increase in gate–source current when large channel currents are flowing in the source–drain direction (negative I_{DS}).

Limiting the gate current to some arbitrary magnitude increases the drain–source voltage drop for large source-to-drain currents in exchange for lower drive losses.

5.3 Reverse conduction

The EM SiC JFET's forward and reverse conduction characteristics are shown in Fig. 6. At lower gate–source voltages, a lower channel voltage drop is observed for reverse conduction compared with forward conduction. Under the thermal characteristics of the test performed, thermal runaway occurs at ~6 A in the forward direction, and 14 A in the reverse direction for a gate–source voltage of 2 V. At the higher gate–source voltage of 3 V, the forward and reverse conduction characteristics are more similar to each other. The reverse conduction characteristic is also shown with the gate driven by a 250 mA constant current source.

When the gate is driven by a 250 mA current source, the channel voltage drop is not substantially different to that observed when the gate is driven with a 3 V voltage source for negative drain currents <10 A in magnitude. For negative drain currents of 11 A and upwards, the difference

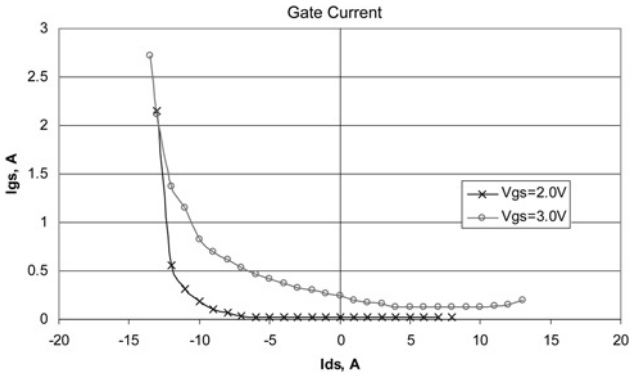

Fig. 5 *Effects of drain current on gate current with fixed gate–source voltage*

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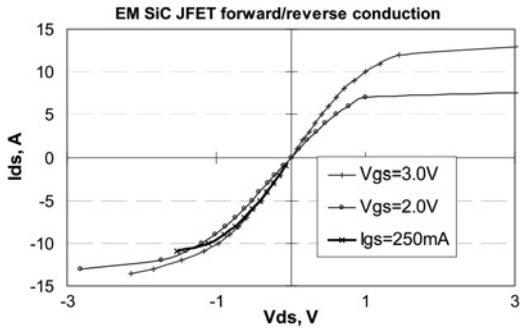

Fig. 6 *Comparison between constant gate current and constant gate voltage*

in channel voltage drop between constant current and constant voltage gate biases becomes more apparent. A trade-off exists between drive losses associated with the excessive gate current that a voltage source bias will deliver and the large conduction losses experienced with a constant current gate drive. A more practical solution is the addition of a diode connected in anti-parallel with the SiC JFET to carry large negative drain currents.

5.4 Reverse recovery-like characteristics

A significant, brief reverse recovery current is observed, caused by capacitive effects. The same test conditions were applied to a MOSFET, hyper-fast diode, SiC Schottky diode and several transistor–diode combinations. Reverse recovery times under these fixed conditions were measured using the methods in [18] and are summarised in Table 1, where Ta is the time between the first zero crossing and the peak of the overshoot current and Tb is the time between the peak of the overshoot current and the next zero crossing. The sum of Ta and Tb is the reverse recovery time, Trr, as defined in [18]. The EM SiC JFET's reverse recovery-like characteristic is significantly faster than that of the much lower voltage silicon MOSFET.

5.5 Performance in proposed boost converter topology

A prototype circuit for the topology in Fig. 2 was designed to boost a DC input of between 0 and 325 V ($230\cdot\sqrt{2}$) to 400 V DC output. This circuit was then constructed to test the mathematical model in Section 3.1.

The prototype is thus operated at a number of discrete DC input voltages (~50–120 V, in 10 V steps), in each case with a DC output voltage of 400 V, to simulate the real circuit at different operating points in one positive mains half-cycle.

The prototype makes use of the JFET driving principles outlined in Section 2.1, utilising pairs of gate drivers to deliver high-current turn-on pulses, continuous gate drive currents and high current, negative gate biases at turn-off. Best practices for circuit layout were followed to further maximise switching transition speeds and minimise ringing and interference.

Table 1 Reverse recovery times for SiC JFET compared with other devices

Device	Ta, ns	Tb, ns	Trr, ns.
SiC JFET	18.0	20.0	38.0
Si MOSFET (600 V)	140.0	29.3	169.3
Si Hyper-fast diode	14.6	9.9	24.5
SiC Schottky diode	13.6	9.1	22.7
SiC JFET & SiC diode	23.0	22.9	45.9

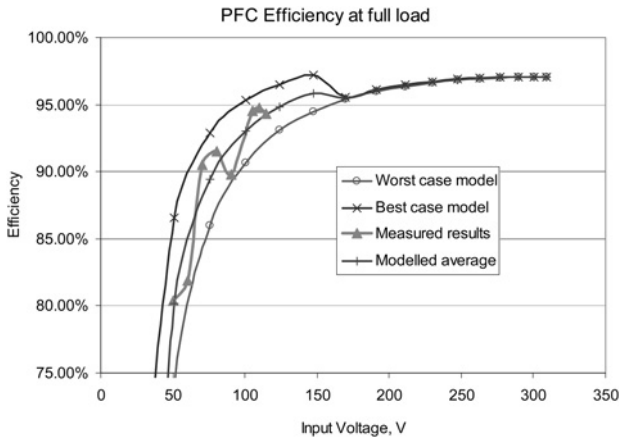

Fig. 7 *Measured and theoretical PFC performance*

The prototype was operated along the same 4 kW peak input power curve used in the mathematical model, up to the maximum level allowed by limitations in the prototype's implementation (~120 V, 500 W). Above this point the prototype circuit was unable to operate reliably, because of shortcomings in the simple feedback control loop used. Conversion efficiency was measured via the input and output voltages and currents. Three measurements were taken at each operating point and averaged to improve accuracy, after allowing the feedback circuitry to settle and thermal equilibrium to be reached. The measured efficiency curve is shown in Fig. 7 along with the modelled performance.

As described in 0, during DCM, the voltage present across each transistor at turn-on varies based on input voltage, conversion power and many parasitic circuit elements, resulting in a varying degree of soft switching. In the measured efficiency curve, these effects are clearly shown by a sinusoidal variation in efficiency between the best and worst case models as expected. Each time the inductor current reached zero during DCM, resonance occurred between the inductor (L1) and parasitic circuit capacitances, resulting in the voltage blocked by Q2 varying with the oscillations. Local maxima in the efficiency curve were confirmed using an oscilloscope as coinciding with Q2 turning on close to local minima in its varying drain–source voltage. Conversely, local minima in efficiency coincided with Q2 turning on near local maxima of drain–source voltage.

Above 180 V, the circuit can be shown mathematically to operate in CCM, resulting in hard switching at all times. This is clearly visible in the decrease in efficiency for the 'best case' model. In practice, the observed switching waveforms confirmed the proximity of the continuous/DCM boundary at the upper end of the measurement range allowed by the prototype's implementation.

6 SiC JFET as a drop-in replacement

To further gauge the relative performance of the EM SiC JFET compared with that of silicon MOSFETs, a test was designed where the EM SiC JFET was retrofitted into the PFC stage of an off the shelf telecommunications rectifier.

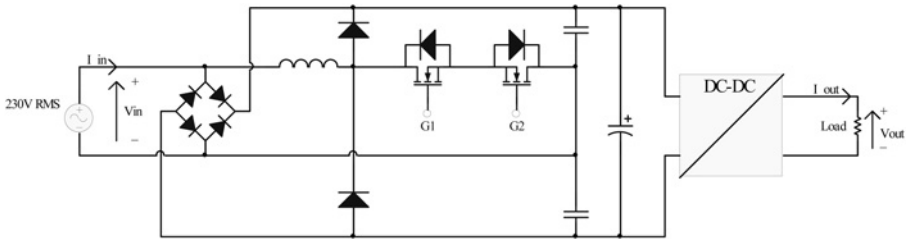

Fig. 8 *Topology of the telecommunications rectifier product's APFC stage*

The telecommunications rectifier contains a dual-stage converter to allow high-efficiency power conversion from 230 V AC to 48 V DC while achieving a high-power factor. The product is typically used to power communications equipment in cellular base stations and digital subscriber line access multipliers. The rectifier product has a single-phase APFC boost circuit at its input, whose underlying topology is shown in Fig. 8, followed by a DC–DC converter. With modifications to the gate drive circuits, the two MOSFETs normally used in the APFC stage can be readily replaced with EM SiC JFETs.

6.1 Measurement techniques for telecommunications rectifier test

To accurately compare the performance of the converter with either EM SiC JFETs or Si MOSFETs, including any differences in drive losses, voltage and currents at the input and output of the converter are measured in a black box approach.

To maximise the precision and accuracy of the results, the input power is measured using a high precision, calibrated Yokogawa WT230 AC power meter. The output voltage and current are measured using high precision Agilent 34 970 A data loggers and a calibrated, temperature-controlled DC shunt. The input voltage is regulated within a 1 V RMS tolerance at all times and a computer is used to acquire all measurements simultaneously, via a general purpose interface bus (GPIB) communications interface. By averaging several repeated measurements for each data point, time-synchronised with each other and the mains, consistent, accurate performance measurements can be acquired.

For comparison purposes, the same telecommunications power converter and measuring equipment is used to test each set of transistors.

6.2 Drop-in replacement results

The power conversion efficiency of the commercial telecommunications power supply was measured at a range of power levels while operating at its nominal AC voltage of 230 V AC. The tests were conducted with 1200 V EM SiC JFETs, followed by the best in class 900 and 600 V silicon MOSFETs available at the time. The test results are summarised in Fig. 9.

The 1200 V SiC JFETs achieve higher conversion efficiency than modern 900 V IPW90R120 silicon MOSFETs, in addition to possessing a superior breakdown voltage.

The 600 V IPW60R099 silicon MOSFETs outperformed the 1200 V SJEP120R125 EM SiC JFETs by a small margin of 3.99 W at the maximum load and 1.9 W at 1 kW. These differences represent 0.2% of output power, suggesting that the EM SiC JFETs perform similarly to

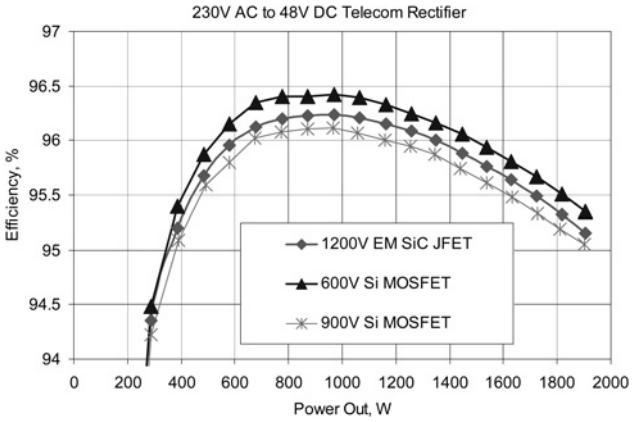

Fig. 9 *Performance of EM SiC JFET against silicon MOSFETs in a real-world application*

600 V silicon MOSFETs, while being capable of blocking 1200 V.

7 Discussion and conclusions

7.1 Reverse blocking characteristics

Despite not possessing a body diode, the EM SiC JFET's diode-like reverse conduction characteristics preclude its use as a single bidirectional blocking device (although bidirectional blocking is easily achieved by the back-to-back connection of two devices).

The voltage drop observed when carrying reversed polarity (source-to-drain) channel currents can be increased with the application of a negative gate–source potential.

In a MOSFET, the body diode typically exhibits poor reverse recovery, resulting in significant switching losses. MOSFET body diodes also exhibit relatively small forward voltage drops compared with faster high-voltage diodes such as SiC Schottky barrier diodes. This makes the connection of a fast diode in anti-parallel to a MOSFET's body diode an impractical solution.

The EM SiC JFET's controllable source–drain voltage drop allows a fast anti-parallel diode to be selected without its forward voltage drop being a significant selection criterion. This characteristic is particularly favourable in high-frequency SR applications and is an advantage that the EM SiC JFET possesses compared with silicon MOSFETs.

7.2 Gate drive energy

Since the EM SiC JFET draws a continuous gate current when biased on, the power required to drive it needs to be considered when designing for maximum conversion efficiency. It was observed during testing that the drain

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current has an effect on the gate current drawn at a particular gate–source voltage. The effect is particularly pronounced when large source–drain currents are flowing. Although the EM SiC JFET is a voltage-controlled device [7] and should be driven accordingly, it is important to limit the maximum continuous gate current if large source–drain currents are expected in the target application, to avoid excessive drive losses.

Tests demonstrated that limiting gate current to 250 mA has only minimal effects on conduction losses for all but the very highest source-to-drain currents that the EM SiC JFET is rated to carry. At these current levels, the voltage drop is sufficient that a carefully chosen anti-parallel diode is likely to offer a reduction in conduction losses regardless of the gate current allowed.

The drive voltage and current limiting resistance chosen have significant effects on EM SiC JFET drive losses. It is important that both be minimised to achieve the lowest possible drive losses. Ideally, the EM SiC JFET would be driven from a current source; however most MOSFET gate drivers approximate good voltage sources, making the circuit proposed a good compromise.

7.3 Reverse recovery and synchronous rectification

The EM SiC JFET's recovery is substantially faster than that of a modern 600 V silicon MOSFET's body diode. The EM SiC JFET's Trr is also less than double that of either a 'hyperfast' silicon diode or a SiC Schottky diode. When an anti-parallel combination of an EM SiC JFET and a diode is used, the combined recovery time remains less than a third that of the silicon MOSFET.

The SiC JFET is therefore likely to exhibit lower reverse recovery losses in SR applications than a silicon MOSFET. An anti-parallel diode is recommended if SR currents above 10 A are expected to flow.

7.4 Real-world performance

In a commercial telecommunications power supply's PFC stage, similar performance was observed between the 1200 V EM SiC JFET, 600 V silicon MOSFETs and 900 V silicon MOSFETs under light load conditions. With increasing load, the losses diverged with the EM SiC JFET performing in between the 600 V silicon MOSFET and 900 V silicon MOSFET. This suggests that conduction losses dominate over switching losses. Close inspection of manufacturers' specifications reveal that the 600 V silicon MOSFET and 1200 V SiC JFET exhibit very similar channel resistances at 25°C. Despite being packaged in the same style of casing, the junction to case thermal impedance of the EM SiC JFET is more than double that of either the 600 or 900 V silicon MOSFET. This is because of the EM SiC JFET's significantly smaller die. Since the EM SiC JFETs were tested in the same circuit as the silicon MOSFETs (electrically and thermally), the higher thermal impedance of the JFETs resulted in a higher junction temperature. The higher operating temperature in turn increased the channel resistance, effectively causing a multiplier effect to the thermal equilibrium junction temperature.

The thermal impedance is clearly one of the EM SiC JFET's largest shortcomings. At the same time, the small die is also responsible for the EM SiC JFET's cost-effectiveness and low capacitances. The small die may also allow the use of smaller packages, resulting in further cost reductions. Smaller packages would also allow a reduction in case to heat sink capacitance and associated EMC noise currents.

7.5 Overall performance

The 1200 V EM SiC JFET achieves performance almost on par with the current best 600 V silicon MOSFETs. When compared with some of the best 900 V silicon MOSFETs, the EM SiC JFET exhibits superior performance in speed, reverse recovery and conduction losses. The EM SiC JFET is thus a preferred choice over the silicon MOSFET in a number of applications where a voltage larger than 600 V must be blocked.

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